

HIGH FREQUENCY MICROMECHANICAL PIEZO ACTUATED DISK RESONATOR

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ABSTRACT

This paper presents the design, simulation, fabrication and testing of a piezo transduced high frequency micromechanical resonator. The resonator is designed to operate in the wine-glass mode and the anchors are optimized to both suppress spurious modes and minimize the energy loss into the substrate. The resonator is fabricated with a simple 4-mask low temperature process from SOI wafer. The highest temperature during the process is 250°C, allowing post-COMS integration compatibility. A prototype resonator with measured diameter of 100 μm was tested in air using non-optimized experimental setup, with measured resonant peaks at 44.97 MHz and 138.5 MHz, which match the simulated result from Ansys®. The quality factor of 35 at 138.5 MHz is extracted, and is expected to be substantially higher if measured in vacuum with calibrated RF cables.

INTRODUCTION

Due to their small sizes, on-chip integration potential, and better performance, micromechanical resonators are attractive as replacements for the off-chip filters and oscillators currently used in communication systems. Significant process has been made in the last decade in this technology, with high quality factors ($>10,000$) in GHz range with impedance matching being the main focuses of current research activities. The state-of-research reported in [1] and [2] a Q factor of 14,600 at frequency of 1.2 GHz. However, the impedance matching between the resonators and signal pickup circuits remained unsolved, and the nanometer-scale capacitive gap required by this approach posed a fabrication challenge. An SOI based high frequency disk resonator was presented in [3], in which a Quality factor of 39,300 at 147.8 MHz was reported. This result was superior than its polysilicon counterpart [4], but the nano-gap remains inevitable for electrostatic transduction. A piezoelectric thin film micromechanical beam resonator was reported in [5], and SOI counterpart of this clamp-clamped beam resonator was demonstrated in [6], although the Q values were high, the frequencies were in the KHz to low MHz range.

In RF range, piezoelectric transduction may provide significant advantages over capacitive transduction, especially in impedance matching, since the admittance ratio between piezoelectrically transduced clamp-clamp beam resonator and electrostatically transduced plate resonator is proportional to the second-order resonant frequency [5]. The current work is motivated by the need to solve the impedance matching problem of capacitively transduced resonator while reaching a frequency and quality factor of the same order. This paper introduces the first wineglass mode disk resonator using piezoelectric transduction to circumvent the nano-gap fabrication requirement and to enable impedance matching. The design, simulation, fabrication and characterization results at the first and second wineglass mode are presented.

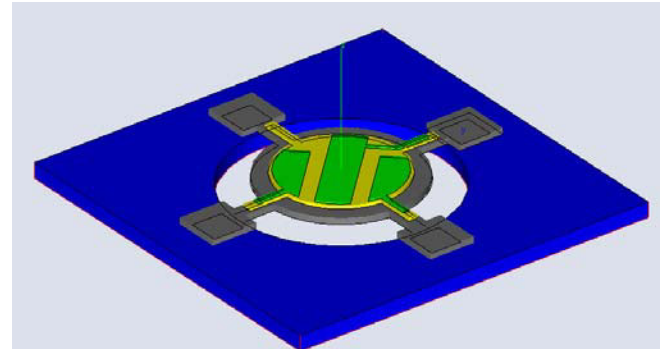


Figure 1. The perspective view of the wine-glass mode resonator design. The resonator is supported by four anchor beams at its quasi-node positions, and the length of the anchor beams is designed to be quarter acoustic wavelength to minimize energy loss. [8]

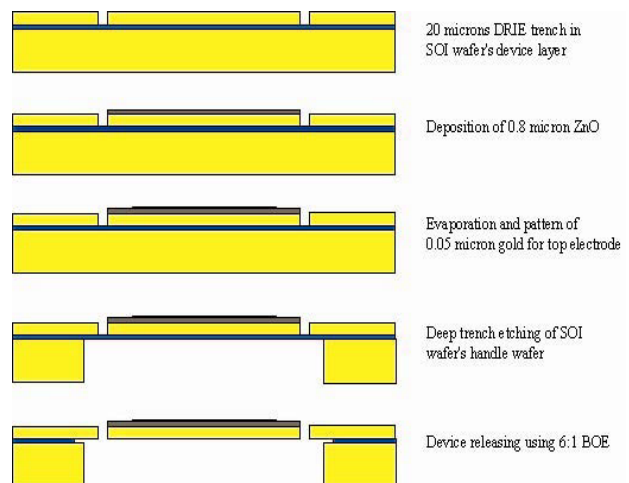


Figure 2. The detailed process flow for the piezo transduced disk resonator. The highest process temperature is 250°C at the zinc oxide sputtering step.

RESONATOR FABRICATION

Figure 1 shows the perspective view of the resonator. This resonator is fabricated with a 4-mask process from SOI wafer, eliminated the need for high-temperature deposition of structural and sacrificial thin films.

The highest processing temperature was the ZnO sputtering at 250°C, which offers the opportunity for post-CMOS integration. Also, the single-crystalline silicon is superior to polysilicon because of its higher material quality factor, lower intrinsic stress,

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and more predictable mechanical and electrical properties. Thin-film zinc oxide is chosen as the piezoelectric transducer for its high electromechanical coupling coefficient and mature fabrication process [7]. A thin layer of gold (500Å) is used for top electrode and the heavily-doped silicon serves as both structure layer and the bottom electrode [8], which simplifies the process by eliminate one step of metal evaporation and patterning. Structural layer is designed to be 20 µm thick to suppress the out-of-plane spurious modes. Figure 2 shows the cross-sectional views of the process flow.

The first masking and etching step defined the resonator, in which 10-µm-wide trenches were etched through the thickness of the <100> device layer of the SOI wafer with inductively coupled plasma (ICP) deep reactive ion etching (DRIE), exposing the buried oxide layer. A thin layer of zinc oxide (0.8 µm) was then deposited by RF sputtering with the Sputtersphere822 system in the USC MEMS group. The zinc oxide was then etched using solution of acetic acid, phosphorus acid and DI water with concentration of 1:1:110. This wet etching process produced substantial undercut and was the main cause for yield loss. 500Å of Gold was evaporated and patterned with lift-off to form the top electrode. The bottom side of the SOI wafer was patterned with double-side alignment and etched through with DRIE to the oxide layer. This backside opening was necessary to facilitate removal of the buried oxide layer with 6:1 Buffered Oxide Etchant (BOE), which was substantially faster than etching from the front side. Two prototypes of the resonators are shown in Fig. 3. Figure 4 shows the side wall profile of the DRIE-etched disk. The scalloping surface roughness was typical of an un-optimized DRIE process, and very likely contributed to surface losses.

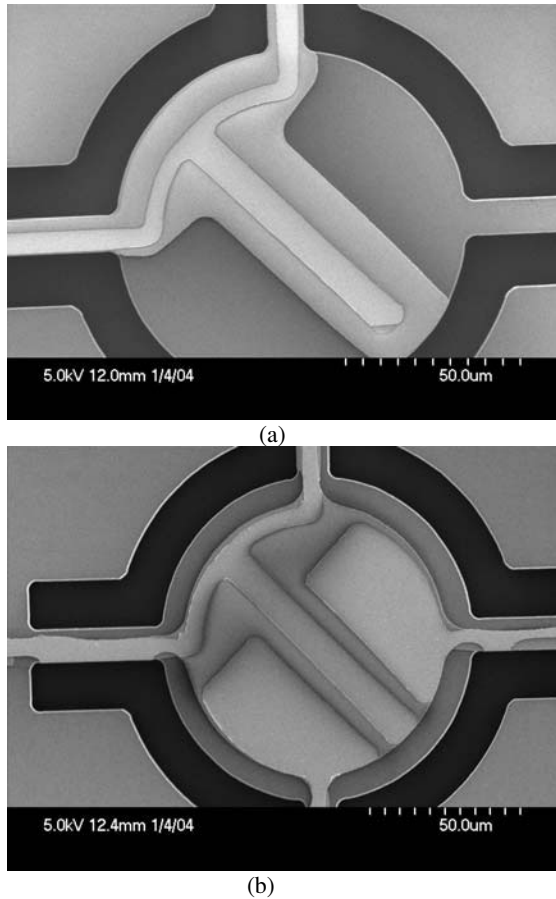


Figure 3. The SEM pictures of 100-µm-diameter resonators in (a) one Port and (b) two-port configuration.

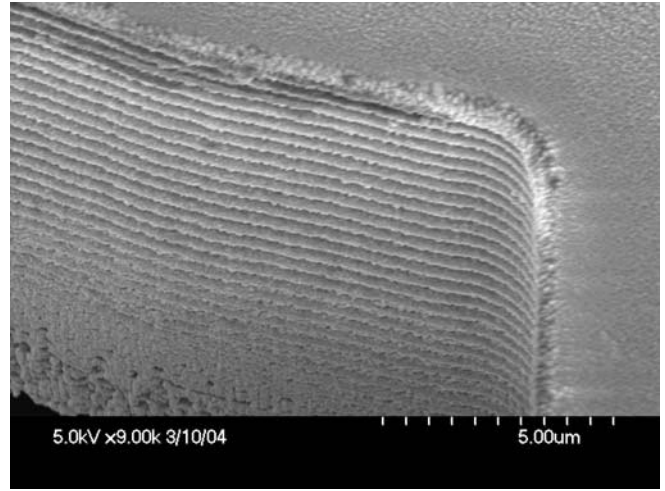


Figure 4. SEM of the side wall profile of the disk resonator. The scalloping surface is typical of some DRIE process, and may likely contribute to surface energy loss.

MEASUREMENT AND SIMULATIONS

The one port resonator with diameter of 100 µm and four supporting beams (10 µm wide by 42.6-µm-long) was tested with HP8753D network analyzer under atmospheric pressure. This initial test setup was not optimized. The uncalibrated DC cables and probes induced significant signal loss and partially contributed to the observed low quality factors. Figure 5 shows the measured microwave reflection coefficient S_{11} . The impedance (Z) was evaluated from the measured S_{11} with:

$$S_{11} = (Z - 50) / (Z + 50)$$

The calculated impedance is plot in Fig. 6. The resonant peaks were determined at zero imaginary impedance, and were 44.97 MHz and 138.5 MHz for the first and second modes, respectively. The quality factors were calculated with the following formula [9]:

$$Q = \frac{f}{2} \frac{\partial Z_{\text{phase}}}{\partial f}$$

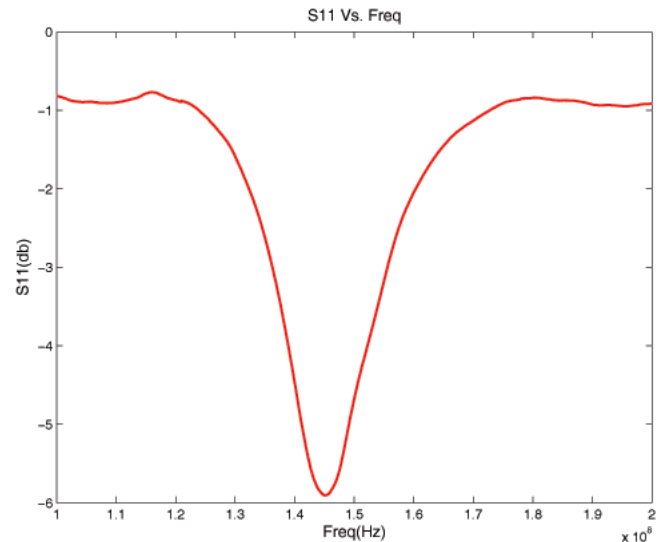


Figure 5. The measured S_{11} from a one port disk resonator.

The evaluated Q values were 3 and 30 for the first and second resonances, respectively.

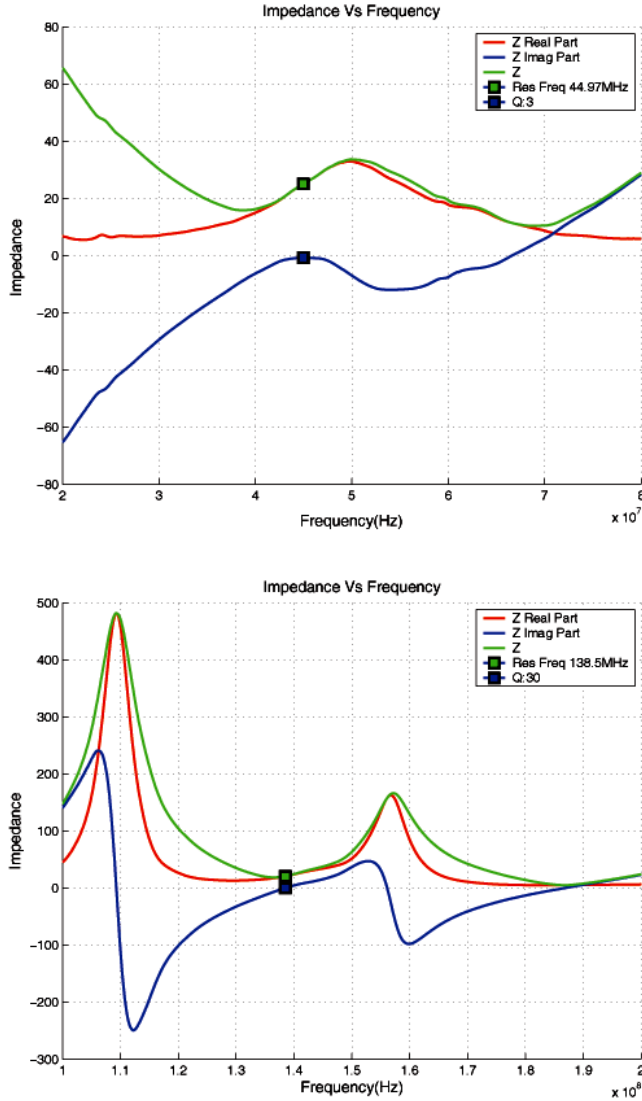


Figure 6. The calculated impedance of the one port resonator with diameter of 100μm at (top) sweeping frequency from 20 MHz to 80 MHz and (bottom) sweeping frequency from 10 MHz to 200 MHz.

The resonator was simulated with Ansys©. The first and second wineglass modes were obtained at 43.5 MHz and 126 MHz, respectively. These simulated results matched the measured resonant peaks well (within 3% and 9%, respectively) and validated the vibration modes. Figure 7 shows the simulation results.

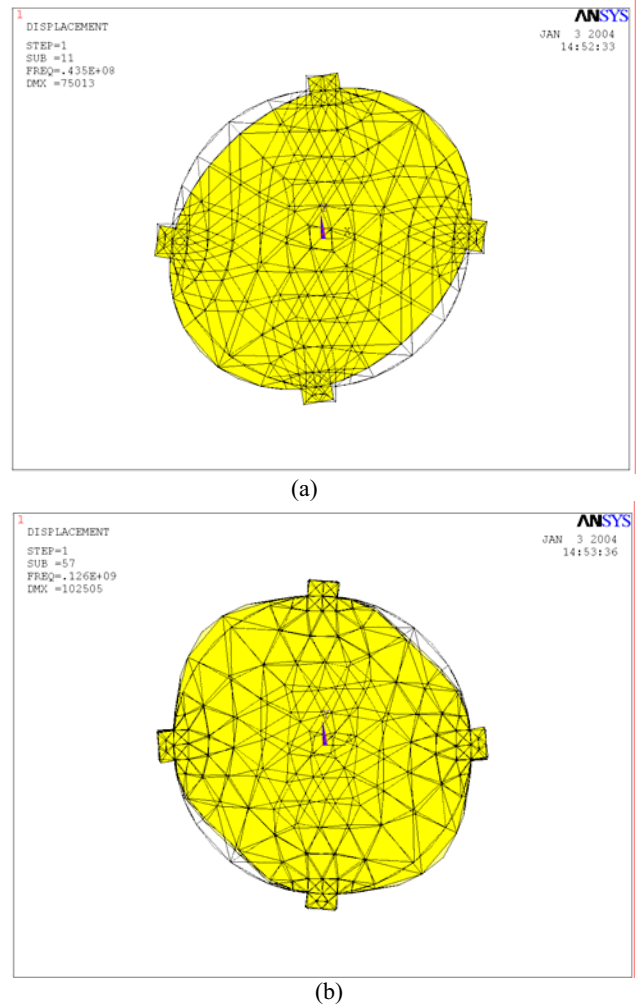


Figure 7. The simulation result of the 100-μm disk resonator at the first and second wineglass resonant modes, which corresponds to resonant frequencies of 43.5 MHz and 126 MHz, respectively.

CONCLUSIONS AND FUTURE RESEARCH

By employing piezoelectric transduction, the nano-gap fabrication required for capacitive transduction is eliminated, and, more importantly, the impedance has been demonstrated for the first time, to match the 50 ohm transmission line at 44.97 MHz and 138.5 MHz. The first-generation devices were fabricated, revealing needs for improvements. The test setup will also be optimized to ascertain more accurate Q values. Future efforts will concentrate on raising the resonant frequencies from VHF to UHF by moderately reducing the diameter and improving Q substantially by optimizing the design and fabrication processes. First, the sidewall scalloping roughness can be substantially reduced by carefully tuning the DRIE process. Further smoothness may be achieved with a brief thermal oxidation and oxide removal with 2% HF, as shown in [10]. Second, the beam design will be improved to enhance Q factors. The current 10-μm width of the supporting beams is overly conservative and thus contributes to energy loss. It will be reduced to level comparable with [3] in future devices. The number of anchor beams should also be reduced, as indicated in [11] and [12]. Third and finally, excessive ZnO at unnecessary location has been proven to contribute to low quality factors and should be removed. It has been demonstrated in

[6] that the quality factor could be improved by a factor of 2 by removing unnecessary ZnO.

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